IN THE CLAIMS:

Listing of claims:

1. (previously presented) A semiconductor device having a non-volatile memory transistor, comprising:

a semiconductor layer;

a floating gate disposed over the semiconductor layer through a first dielectric layer as a gate dielectric layer;

a second dielectric layer that contacts at least a part of the floating gate and is capable of functioning as a tunneling dielectric layer;

a control gate formed over the second dielectric layer; and

source and drain regions in the semiconductor layer,

wherein a conduction layer is provided above the floating gate, and the conduction layer entirely overlaps the floating gate.

2. (original) A semiconductor device having a non-volatile memory transistor according to claim 1, wherein the conduction layer outwardly protrudes from an end of the floating gate as viewed in a plan view, and a width of a portion of the conduction layer that outwardly protrudes from the end of the floating gate as viewed in a plan view is 0.5 μm or smaller.

3. (original) A semiconductor device having a non-volatile memory transistor according to claim 1, wherein a side end of the conduction layer formed above the floating gate and an end of the floating gate are aligned with each other.

4. (original) A semiconductor device having a non-volatile memory transistor according to claim 1, wherein a width of the conduction layer above a region other than a region where the floating gate is formed is narrower than a width of the conduction layer above the region where the floating gate is formed.

5. (original) A semiconductor device having a non-volatile memory transistor according to claim 1, wherein the conduction layer is electrically connected to the semiconductor layer.

6. (currently amended) A semiconductor device having a non-volatile memory transistor device as in claim 28, wherein the conductive material includes a plurality of conduction layers formed at different levels above the floating gate, and the floating gate is entirely overlapped by the plurality of conduction layers as viewed in a plan view.

7. (currently amended) A semiconductor device having a non-volatile memory transistor according to claim 6, wherein at least one of the conduction layers outwardly protrudes from an end of the floating gate as viewed in a plan view, and a width of a portion of the at least one of the conduction layers~~layer~~ that outwardly protrudes from the end of the floating gate as viewed in a plan view is 0.5 μm or smaller.

8. (original) A semiconductor device having a non-volatile memory transistor according to claim 6, wherein a side end of the at least one of the conduction layers and an end of the floating gate are aligned with each other.

9. (original) A semiconductor device having a non-volatile memory transistor according to claim 6, wherein the conduction layer is electrically connected to the semiconductor layer.

10. (canceled)

11. (previously presented) A semiconductor device having a non-volatile memory transistor, comprising a non-volatile memory transistor including a semiconductor layer, a floating gate disposed above the semiconductor layer, and a control gate formed above the floating gate,

wherein a conduction layer is provided above the non-volatile memory transistor and at least a portion of the conduction layer is located vertically above the floating gate along the entire length of the floating gate, and

a width of the conduction layer located vertically above the floating gate is formed to be greater than a width of the floating gate.

12. (original) A semiconductor device having a non-volatile memory transistor according to claim 11, wherein a width of the conduction layer located other than vertically above the floating gate is formed to be smaller than a width of the conduction layer located vertically above the floating gate.

13. (original) A semiconductor device having a non-volatile memory transistor according to claim 12, wherein the conduction layer is a wiring layer.

14. (original) A semiconductor device having a non-volatile memory transistor according to claim 13, wherein the wiring layer is a lowermost wiring layer.

15. (previously presented) A semiconductor device having a non-volatile memory transistor as in claim 29, wherein the conductive material includes a plurality of conduction layers provided above the non-volatile memory transistor, and

at least one conduction layer among the plurality of conduction layers is provided vertically above the floating gate at least in a region where the control gate is not disposed vertically above the floating gate.

16. (original) A semiconductor device having a non-volatile memory transistor according to claim 15, where the conduction layers are wiring layers.

17. (previously presented) A semiconductor device having a non-volatile memory transistor according to claim 15, further comprising:

a first dielectric layer that defines a gate dielectric layer disposed between the semiconductor layer and the floating gate;

a second dielectric layer that contacts at least a part of the floating gate and is capable of functioning as a tunneling dielectric layer; and

source and drain regions in the semiconductor layer.

18. (previously presented) A semiconductor device having a non-volatile memory transistor according to claim 1, wherein the non-volatile memory transistor comprises a first circuit region, and wherein the semiconductor device further comprises a second circuit region, wherein the first circuit region and the second circuit region are formed in a sea of gates structure.

19. (original) A semiconductor device having a non-volatile memory transistor according to claim 18, wherein the second circuit region includes at least a logic circuit.

20. (canceled)

21. (original) A semiconductor device having a non-volatile memory transistor according to claim 15, wherein the non-volatile memory transistor comprises a first circuit region, and wherein the semiconductor device further comprises a second circuit region mix-mounted therein.

22. (original) A semiconductor device having a non-volatile memory transistor according to claim 21, wherein the second circuit region includes at least a logic circuit.

23. (canceled)

24. (previously presented) A method for manufacturing a semiconductor device having a non-volatile memory transistor, comprising:

forming a first dielectric layer comprising a gate dielectric layer on a semiconductor substrate;

forming a floating gate over the gate dielectric layer;

forming a second dielectric layer that contacts at least a part of the floating gate and is capable of functioning as a tunneling dielectric layer;

forming a control gate over the second dielectric layer;

forming source and drain regions in the semiconductor substrate; and

forming a conduction layer above the floating gate so that a portion of the conduction layer is positioned vertically above the floating gate, where the portion of the conduction layer overlaps the entire floating gate.

25. (canceled)

26. (previously presented) A method for manufacturing a semiconductor device having a non-volatile memory transistor, comprising:

forming a floating gate above a semiconductor layer;

forming a control gate that extends above a portion of the floating gate; and

forming a conduction layer vertically above the floating gate at least in a region where the control gate is not disposed vertically above the floating gate, and

forming the conduction layer to have a width greater than that of the floating gate in a region where the conduction layer is disposed vertically above the floating gate.

27. (previously presented) A method for manufacturing a semiconductor device having a non-volatile memory transistor as in claim 30, wherein the conductive material comprises a plurality of conduction layers formed vertically above the floating gate at least in a region where the control gate is not disposed vertically above the floating gate.

28. (previously presented) A semiconductor device having a non-volatile memory transistor, comprising:

a semiconductor layer;

a floating gate disposed over the semiconductor layer through a first dielectric layer as a gate dielectric layer;

a second dielectric layer that contacts at least a part of the floating gate and is capable of functioning as a tunneling dielectric layer;

a control gate formed over the second dielectric layer; and

source and drain regions in the semiconductor layer,

wherein a conductive material is formed above the floating gate, and the floating gate is entirely overlapped by the conductive material as viewed in a plan view.

29. (previously presented) A semiconductor device having a non-volatile memory transistor, comprising a non-volatile memory transistor including a semiconductor layer, a floating gate disposed above the semiconductor layer, and a control gate formed above the floating gate, the floating gate including an upper surface, wherein a conductive material is positioned vertically above the entire upper surface of the floating gate.

30. (previously presented) A method for manufacturing a semiconductor device having a non-volatile memory transistor, comprising:

forming a floating gate above a semiconductor layer, the floating gate including an upper surface;

forming a control gate above the floating gate,

providing a conductive material above the non-volatile memory transistor, and

positioning the conductive material vertically above the entire upper surface of the floating gate.

31. (canceled)